ABSTRACT OF THE DISCLOSURE

An apparatus may include an ECC check circuit configured to detect an ECC error in response to an access to first data in a memory and a microcode unit. The microcode unit is coupled to receive an indication that the ECC check circuit has detected the ECC error. In response to the indication, the microcode unit is configured to dispatch a microcode routine stored by the microcode unit. The microcode routine includes instructions which, when executed, correct the ECC error in the memory. In another embodiment, a processor includes the microcode unit and execution circuitry. A method is also contemplated. An access is performed to first data in a memory. An ECC error is detected in response to the access. A microcode routine stored by a microcode unit is dispatched in response to the detecting of the ECC error. The microcode routine includes instructions which, when executed, correct the ECC error in the memory.